ECE 483 Project 4 (Multiply unit)

IPC Integrated Processor Corporation is currently doing well selling SEPs, However they are facing new competition. There are several new processors on the market that have similar prices and performance to the SEP, however, they also have a multiply instruction, which makes them a much more attractive processor for new products.

In order to combat this new competition, instead of waiting for there next generation processor to be finished, a stop-gap measure must be taken: add a multiply instruction to the SEP.

In order to support the new multiply instruction, two new registers, and a multiply unit must be added. The two new registers are Product High Byte and Product Low Byte. In this way, multiplying two sixteen bit numbers will give a 32 bit result, half in PHB and half in PLB.

The following instructions will also need to be added (You will need to replace one of the memory reference instructions with the MUL instruction)

MUL: (Multiply)

PHB:PLB = accumulator * M[address]

GHB: Get High Byte
AC = PHB

GLB: Get Low Byte
AC = PLB

Note that average performance should not be sacrificed for the sake of having a multiply instruction. Simply stated, the clock speed of the SEP before and after the modification should be roughly the same (This implies that the multiply should take several clock cycles).

Your job, should you choose to accept the challenge is to implement the above scheme in the SEP. You should design your modified SEP in Verilog. You should also write a report and give a presentation that gives specific details of your changes.