ECE 483 Project 3 (Interrupts)

In the SEP and Data unit you will need to implement the input and output registers.

In the Control Unit you will need to do some extra work on the interrupts. An interrupt on either the fgi or fgo set lines should bring the processor out of halt (but only if the IEN flag is set). One particularly problematic aspect of this is that a naive implementation of this feature will by default execute the instruction immediately after the halt instruction, then execute the interrupt routine. Your implementation **SHOULD NOT DO THIS**. For your test bench you should execute the instructions given in the Pre-Lab, then sometime after the processor successfully halts, you should drive either set_fgi or set_fgo high and observe the interrupt cycle.

To test your SEP, you need to write an Interrupt Service Routine. The ISR should be located at $100 in memory. The function of this ISR should be to take the input register, copy it's contents to address $E0F and then to the output register. Then return control back to the main program. One Caveat though. If the Interrupt occurs after the HLT instruction, the interrupt will wake the SEP up. When the ISR returns control back to the main program it will start to execute the instruction after the HLT. To fix this, make an instruction immediately after the HLT instruction a BUN back to the HLT instruction. For a detailed description of what an ISR should look like, read the "Program Interrupt" section of 6-8 on pages 205-208 of the Mano Text. Make sure you save the Accumulator value and restore it after the interrupt. Similarly make sure you re-enable the IEN bit at the end of the ISR. You need to include annotated waveforms of the ISR executing.

Your lab report should contain the specifics of how you implemented the interrupts and any problems you encountered when you implemented them.